UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,425	08/22/2003	Emrah Acar	AUS920030496US1	9656

7590 04/06/2006

Richard F. Frankeny
1201 Main Street
P.O. Box 50784
Dallas, TX 75250-0784

EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 04/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No. 10/646,425	Applicant(s) ACAR ET AL.
	Examiner Helen Rossoshek	Art Unit 2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/646,425 filed 08/22/2003 and amendment filed 01/11/2006.

2. Claims 1-20 remain pending in the Application.

3. Applicant's arguments have been fully considered but they are not persuasive.

Drawings

4. The drawings are objected to because Figures 4 and 5 have errors in the labeling, such as item 402 is marked as "Max Leakage" in the Figure 4, while named as "average" in the Specification on the page 10, line 17. Figure 5 has the same problem with labeling item 503. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the

examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Cohn et al. (US Patent 6,711,719).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

With respect to claims 1 and 11 Cohn et al. teaches a method for designing an integrated circuit (IC) having IC parameters including process, circuit, and environmental design parameters (col. 1, ll.8-12), a computer program product for determining an average macro leakage power sensitivity for an IC parameter, the computer program product embodied in a machine readable medium, including

programming for a processor, the computer program comprising a program of instructions for performing the program steps (col. 22, ll.44-48), comprising the steps of: using design tools to layout and configure circuit macros making up the IC as shown on the Figs. 2 and 3, wherein a layout of the logic network 10(portion of the integrated circuit) including logic blocks 42, 52 and 62 (circuit macros) are depicted and for defining a cut 35 to configure the blocks (col. 8, ll.61-63; col. 9, ll.46-50); determining a leakage power for each of the circuit macros within determining the information about a power leakage for each block (macro) (col. 3, ll.5-6); determining average leakage power sensitivities for the circuit macros to variations in the IC parameters within sensitivity analysis in the form of a derivative of leakage power (average leakage power) (col. 11, ll.59-67), wherein sensitive analysis includes evaluation of the potential network changes (parameter changes); selecting first parameters from the IC parameters in response to analyzing the average leakage power sensitivities by selecting the changes (parameters) of the network (macros) as the portion of the integrated circuit with evaluation of the benefit of the changes in term of variations of the leakage power derivative (col. 12, ll.16-26); and reducing a leakage power for one or more selected circuit macros of the circuit macros of the IC by modifying one or more of the first parameters within changes in the network (macro) in the arbitrary manner to find an improvement (reducing leakage power) in the optimization objective (col. 12, ll.17-22; col. 3, ll.49-50).

With respect to claims 2-10 and 12-20 Cohn et al. teaches:

claims 2 and 12: wherein the circuit macros are classified as timing-noncritical circuit macros and timing-critical circuit macros, wherein the timing-noncritical circuit macros may have the IC parameters modified without significantly affecting an overall IC performance as shown on the Fog. 8a, wherein the gates (macros) are classified by size, and size is proportional to the timing criticality (gates with the bigger size are timing–critical circuits), and the leakage power is proportional to the circuit size (timing-critical circuits) (col. 17, ll.50-53; ll.57-58);

claims 3 and 13: wherein the one or more selected circuit macros correspond to timing-noncritical circuit macros within improved conventional method to reduce current leakage (col. 2, ll.18-23), wherein conventional method includes selecting a portion of the non-timing critical logic path (col. 1, ll.22-24);

claims 4 and 14: further comprising the step of determining a power dissipation margin as a difference between a first design power dissipation for the IC and a second power dissipation determined for the IC after the step of reducing the leakage power (col. 20, ll.59-67);

claims 5 and 15: further comprising the step of redesigning one of the circuit macros corresponding to the timing-critical circuit macros using the power dissipation margin to improve a performance of the redesigned circuit macro while keeping the overall IC power substantially equal to or below the first design power dissipation for the IC as shown on the Figs. 8a and 8b, wherein change in the design of the logic network 159 (macro) is depicted, such as adding one more input to the gate GZ, which is timing

critical circuit (since has a bigger size=2) and has the largest leakage power (col. 18, ll.14-16; ll.30-34);

claims 6 and 16: wherein the average leakage sensitivity is determined by a method comprising the steps of: determining occurrence probabilities for each input node of the circuit macros as shown on the Figs. 10a and 10b, wherein node probabilities for net X shown on the Fig. 8a is depicted (col. 18, ll.8-10); calculating state occurrence probabilities for each cell within the circuit macros within determining the probability of each input condition for each gate (cell) in the logic network 150 (macro) shown on the Fig. 8a; retrieving predetermined leakage data and leakage sensitivity data as a function of the IC parameters for cell inputs for the circuit macros from the cell library within replacing the cell (gate) in the logic network (macro) with another cell (col. 14, ll.36-38), as a result of the sensitivity analysis (col. 14, ll.21-23), wherein the information about replacement cell is retrieved from the library (col. 14, ll.45-49); calculating an average leakage current for the circuit macros in response to the leakage data from the retrieving step, the occurrence probabilities for each of the input nodes of the circuit macro, and the state occurrence probabilities of each cell within the circuit macros within computation a leakage derivative for each gate as shown on the Fig. 5 (col. 13, ll.3-8; col. 12, ll.1-5); calculating an average leakage sensitivity for each circuit macro corresponding to each of the IC parameters in response to the leakage sensitivity data from the retrieving step, the occurrence probabilities for each of the input nodes of the circuit macro, and the state occurrence probabilities of each cell within the circuit macros within sensitivity analysis in the form of a derivative of leakage power (average

leakage power) (col. 11, ll.59-67), wherein sensitive analysis includes evaluation of the potential network changes (parameter changes) (col. 13, ll.1-3); and saving average leakage current sensitivity data for each parameter for each circuit macro for use in optimizing the IC design within binary decision diagram to store the probability occurrence of states and power leakage (col. 2, ll.59-63; col. 2, ll.67; col. 3, ll.1-5, ll.13-18, ll.29-33).

claims 7 and 17: wherein the leakage data and the leakage sensitivity data for the IC parameters for the cell inputs are predetermined by using circuit analysis and circuit simulation tools (col. 4, ll.21-24);

claims 8 and 18: wherein the step of calculating the average leakage current uses a method comprising the steps of: multiplying leakage currents for each logic state of each node of each cell of the circuit macro times corresponding logic state occurrence probabilities for each of the nodes generating a node leakage current for each node of each cell as demonstrated by calculation of the expected leakage of the gate with input probabilities p1 and p2 (col. 13, ll.9-20; col. 17, ll.60-63); summing the node leakage current across each node of the cell generating cell leakage currents (col. 13, ll.22-25); and summing the cell leakage currents across each cell generating the average macro leakage current by calculating the total leakage derivative of the net (col. 13, ll.25-26).

claims 9 and 19: of calculating the average leakage sensitivity for a parameter P of the IC parameters uses a method comprising the steps of: multiplying a leakage sensitivity for the parameter P for each logic state of each node of each cell of the circuit macro times corresponding logic state occurrence probabilities for each of the nodes

generating a node leakage sensitivity for each node of each cell (col. 13, ll.47-49); summing the node leakage sensitivities across each node of the cell generating a cell leakage sensitivity for the parameter P (col. 13, ll.49-55); and summing the cell leakage sensitivities across each cell of the macro generating the average macro leakage sensitivity (col. 13, ll.49-59);

claims 10 and 20: further comprising the step of outputting the saved leakage sensitivity data during IC design in response to a designer request to evaluate affects of modifying the IC parameters to reduce a macro leakage current (col. 13, ll.60-67).

Remarks

7. In the remarks Applicant argues in substance:

A: Nowhere does Cohn teach or suggest the step of using leakage power sensitivity analysis of process, circuit and environmental design parameters of an IC as recited in claim 1 of the present invention.

B: Cohn does not teach or suggest classifying circuit macros whose IC parameters have been determined, as circuit macros that may have these IC parameters adjusted without affecting an overall IC performance.

C: Nowhere does Cohn et al. mention using the IC parameters of Claim 1 to reduce leakage, wherein timing non-critical circuit macros are selected to have their IC parameters modified based on a leakage sensitivity analysis of these parameters as it was discussed.

D: While the present invention and Cohn et al. both determine a change in power dissipation, the determination is done after two completely different methods of reducing leakage power.

E: Cohn describes adding an input to a high leakage gate to reduce the leakage of that gate not to improve its performance as recited in Claim 5.

F: ". . . a step of calculating state occurrence probabilities for each cell within the circuit macros, this step is in addition to the steps not taught by Cohn".

G: Cohn does not teach or suggest using simulation to determine leakage power sensitivity to the IC parameters.

8. Examiner respectfully disagrees for the following reasons:

As to A Cohn et al. discloses **sensitivity analysis** to guide the optimization process and evaluating potential **network changes** (col. 11, ll.59-63), in addition to a **probabilistic analysis** for reducing the power leakage (col. 2, ll.34-35) in the improved method for power leakage reduction control in logic circuits and mechanism for finding leakage probabilities during synthesis to modify the network (macro) (col. 2, ll.36-38), wherein, as shown on the Fig. 6 and described in col. 15, ll.13-25, the network changes are related to the parameters of the network, such as factoring a gate (process parameters), retiming transformation, moving gate to a new location (topology parameters), changing a routing of net (macro), including temperature and power supply (col. 17, ll.54-56; col. 11, ll.44-46) and sensitivity analysis performs sensitivity measure on each net to calculate the leakage current (col. 13, ll.55-59).

As to B Cohn et al. teaches an improved method for power leakage reduction control in logic circuits, which based on passive threshold voltage control method, which typically comprises **selecting** a portion of the **non-timing critical logic paths** (timing non-critical circuit macros) with using higher threshold voltage (as IC parameter) to reduce leakage current (power leakage) without significantly affecting IC performance (col. 1, ll.20-24).

As to C Cohn et al, discloses an improved method for power leakage reduction control in logic circuits and than process reducing the power leakage for **selected** gates as **non-timing critical logic paths** (macros) during **sensitivity analysis** of the IC parameters (e.g. **threshold voltage**) as was mentioned above, wherein gates (macros) are classified by their sizes (col. 17, ll.57-58).

With respect to D as it was established above in response to the argument A Gohn et al. discloses performing sensitivity **analysis** in addition to a probabilistic analysis for reducing the power leakage (col. 12, ll.27-30). Therefore determination of the total effect, on the power leakage of the circuitry (col. 11, ll.64-65) is performed by the same method as claimed in the instant Application.

As to E Cohn discloses change in the design of the logic network 159 (macro) is depicted, such as adding one more input to the gate GZ, which is timing critical circuit (since has a bigger size=2) and has the largest leakage power (col. 18, ll.14-16; ll.30-34) as shown on the on the Figs. 8a and 8b, wherein reducing power leakage leads to reducing area, **improving circuit performance** etc. (col. 4, ll.30-31).

As to F Cohn et al. teaches computing for each input of a gate the change on the state probability of the gate output (probability of that state occurring) (col. 12, ll.60-61), wherein **probability of that state occurring** is used later for computing an average power leakage for each gate (col. 17, ll.60-63).

As to G Cohn et al., as was mentioned above, discloses **sensitivity analysis** to guide the optimization process and evaluating potential **network changes** (col. 11, ll.59-63), in addition to a **probabilistic analysis** for reducing the power leakage (col. 2, ll.34-35) in the improved method for power leakage reduction control in logic circuits and mechanism for finding leakage probabilities during synthesis to modify the network (macro) (col. 2, ll.36-38; col. 12, ll.27-30), wherein simulated annealing methods are also applied (col. 11, ll.33; col. 4, ll.21-24).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
Primary Examiner
Technology Center 2800